Performance Enhancement in a Two-Stage Amplifier with Positive Capacitive Feedback Compensation

This paper presents a two-stage amplifier with positive capacitive feedback compensation and enhanced performance in 0.18μm CMOS process. In this type of amplifier, unlike the Miller compensated two-stage amplifiers, dominant pole is located at the output of the amplifier. So, phase margin (PM) improves if the capacitive load is increased. Effect of the non-dominant pole is reduced by the left half plane zero, which is introduced by the positive capacitive feedback network. In this work, higher gain bandwidth (GBW), higher slew rate, and also higher common mode rejection ratio (CMRR) are achieved, by using a new structure. The proposed amplifier improves low frequency CMRR by 34% (16dB), slew rate by 5% and GBW by 37.3%. For 1.8V supply voltage, DC gain and power consumption are 73.4dB and 88μw, respectively. Also, low frequency CMRR and power supply rejection ratio are 143 and 44.7dB, respectively. GBW, PM, and slew rate for a 5pF capacitive load are 131MHz, 3.26°, and 31 V/μs, respectively. Moreover, 1.1% settling accuracy for a 0.5V input signal in unity gain configuration is 74ns.

Amplifier; high gain; positive capacitive feedback compensation; CMRR; PSRR;