Module-based Synthesis of Behavioral Verilog Descriptions to Asynchronous Circuits

In this paper we present an automatic design tool for synthesizing Verilog behavioral description of an asynchronous circuit into delay insensitive presynthesized library modules, using syntax directed techniques. Our design tool can also generate appropriate output to support implementing the circuit on ASICs and LUT-based FPGAs and rapid prototyping of the asynchronous circuit is readily available.

Keywords: Design, Languages