A new architecture is proposed in which with respect to the conventional successive approximation register (SAR) analog-to-digital converter (ADC), the switching power and capacitor area are significantly reduced without an appreciable increase in digital complexity. In the proposed scheme, the threshold voltage for each comparison is divided into two parts where producing these two parts consumes appreciably less switching energy and requires less total capacitance than the conventional one. With respect to the conventional scheme, the switching power and total capacitance of the proposed SARADC for 10-bit resolution is reduced by more than 78% and 4%, respectively.