This paper presents a novel model and method for synthesis of parallel hierarchical finite state machines (PHFSM) that permit to implement such algorithms, which are:

1) composed of modules;
2) the modules can be activated from other modules;
3) more than one module can be activated in parallel. The synthesis involves three basic steps: 1) conversion of a given specification to special state transition diagrams; 2) use of the proposed hardware description language templates; 3) synthesis of the circuit from the templates. The results of experiments have proven the effectiveness and practicability of the proposed technique.

Keywords: Hierarchy, recursion, programming techniques, hardware accelerators

Link to the paper in Civilica:
https://www.civilica.com/Paper-ICEE21-ICEE21_401.html