Design of An Energy-Efficient Baseband Processor for Implementation of a DVB-S2 Baseband Demodulator based on a low power DSP

This paper presents the design and implementation of a baseband demodulator for DVB-S2 satellite receivers. In order to meet the requirements of different complex and multidomain signal processing stages of the DVB-S2 baseband signal flow, the presented architecture is based on efficient fixed-point implementation of the various demodulation algorithms and on the use of a dynamic time-sharing scheduler for the various DSP software tasks. This paper proposes a low-power high throughput digital signal processor (DSP) for baseband processing in wireless terminals. It builds on our earlier architecture—Signal Processing On Demand Architecture (SODA) which is a four-processor, 32-lane SIMD machine. SODA has several shortcomings including large register file power, wasted cycles for data alignment, etc., and cannot satisfy the higher throughput and lower power requirements of emerging standards. We propose SODA-II, which addresses these problems by deploying the following schemes: operation chaining, pipelined execution of SIMD units, staggered memory access, and multicycling of computation units. The prototyping of the demodulator and its verification in the design of a complete digital DVB-S2 satellite receiver using a versatile testbed is also presented.

Keywords: DVB-S2, Baseband Processor, SODA, SIMD, DSP

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