A Speed Controller System Based on FPGA for High Speed Train

The development of the railway technology, as a leading transportation technology, requires more and more efficient, intelligent and faster subsets. High speed trains, which are the heart of the railway transportation, play a major role in this field. To achieve a reliable and safe high-speed transportation system, the intelligent controllers are always preferred to human supervisor. In order to realize intelligent controllers, beside the processors, the field programmable gate arrays (FPGAs) can be used. The FPGAs are interesting due to low non-recurring engineering (NRE) costs, their reconfiguration capability, and computational efficiency benefits over general purpose processors. A very complex control algorithm can be implemented into FPGA and its run-time can be considerably reduced based on parallel processing hardware circuit. This paper proposes a new architecture of an FPGA based speed controller for high speed trains. According to the proposed architecture, a real system has been constructed based on Altera FPGAs. The proposed approach requires 3\% of FLEX EPF1K240 and it can operate with maximum frequency of 61 MHz. The simulation and implementation results validate the efficiency and functionality of the proposed architecture.

Keywords: high speed train, automatic train control system, speed controller, FPGA