A Low-Power and Low-Energy 1-Bit Full Adder Cell Using 32nm CNFET Technology Node

Full adder cell is often placed in the critical path of other circuits. Therefore it plays an important role in determining the entire performance of digital system. Moreover, portable electronic systems rely on battery and low-power design is another concern. In conclusion it is a vital task to design high-performance and low-power-full adder cells. Since delay opposes against power consumption, we focus on Power-Delay Product (PDP) as a figure of merit. In this paper using carbon nanotube field effect transistors (CNFETs) a novel low power and low PDP 1-bit full adder cell is proposed. The novel cell is based on capacitive threshold logic (CTL) and to strengthen its internal signals transmission gates (TGs) are applied. Using both CTL and TG techniques lead to achieving low power consumption full adder cell. Intensive simulations with 23 nm technology node using Synopsys HSPICE with regard to different power supplies, temperatures, output loads, and operating frequencies are performed. All simulations confirm the superiority of the proposed cell compared to other state-of-the-art cells.

Keywords: Nanoelectronics, Carbon Nanotube Field-Effect Transistor (CNFET), Full Adder, Low Power, Low Energy

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